Indraprastha College for Women
University of Delhi

Course Name:	B.Sc.(H) Computer Science
Paper Title:	Computer System Architecture
Unique Paper Code:	2342011102
Semester:	Ist
Faculty(s):	Ms. Priyanka Gupta
Year:	2025

Work Plan

Unit No.	Learning Objective	Lecture No.	Topics to be Covered
I	**Unit 1:** Digital Logic Circuits	1	**Ch 1: Digital Logic Circuits** Digital Computers
		2	Logic Gates
		3	Boolean Algebra
		4	Karnaugh Maps (up to three variable K-Maps)
		5	Combinational Circuits
		6	Flip Flops Sequential Circuits (up to pg. 28)
II	**Unit 2:** Digital Components (Fundamental building blocks)	7	Ch 2: Digital Components Decoders
		8	Decoders
		9	Encoders
		10	Multiplexers
		11	Memory Unit
		12	Ch 4: Register Transfer and Micro-operations
		13	4.4 (up to fig. 4.7)
		14	4.4 (up to fig. 4.7)
		15	4.4 (up to fig. 4.7)

III		16	Data Types

	Unit 3: Data Representation and Basic Computer Arithmetic	17	Data Types
		18	Complements
		19	Complements
		20	Fixed Point Representation
		21	Fixed Point Representation
IV	Basic Computer Organization and Design	22	Ch 5: Basic Computer Organization and Design 5.1 Instruction Codes
		23	5.2 Computer Registers
		24	5.3 Computer Instructions
		25	5.3 Computer Instructions
		26	5.4 Timing and Control (up to pg. 137)
		27	5.5 Instruction Cycle
		28	5.5 Instruction Cycle
		29	5.6 Memory Reference Instructions
		30	5.6 Memory Reference Instructions
		31	5.7 Input Output and Interrupt
		32	Ch 9: Pipeline and Vector Processing 9.2 Pipelining
		33	Ch 9: Pipeline and Vector Processing 9.2 Pipelining Numericals
V	Unit 5: Processors	34	Ch 8: Central Processing Unit 8.1 Introduction 8.2 General Register Organization
		35	8.3 Stack Organization (up to pg. 247),
		36	8.5 Addressing Modes
		37	8.8 RISC (only characteristics, i.e., pg. 282 – 284)
		38	Ch-7: Multicores, Multiprocessors, and Clusters 7.1 (page 632-Introduction of Multicore Processor) [Ref 2]

		39	7.7 (page 654-656) Characteristics of GPU Vs. CPU [Ref 2]
VI	Unit 6: Memory and Input-Output Organization	40	Ch 11: Input Output Organization 11.2 Input Output Interface (up to pg. 389, excluding example)
		41	11.4 Modes of Transfer
		42	11.6 DMA
		43	Ch 12: Memory Organization 12.1 (up to pg-446)
		44	Revision & pyqs
		45	Revision & pyqs

Syllabus		
S. No.	**Unit Name**	**Contact Hours/ No. of Lectures***
1	**Unit 1:** Digital Logic Circuits	6
2	**Unit 2:** Digital Components (Fundamental building blocks):	5
		4
3	**Unit 3:** Data Representation and Basic Computer Arithmetic	6
4	**Unit 4:** Basic Computer Organization and Design	10
		2
5	**Unit 5:** Processors:	4
		1
6	**Unit 6:** Memory and Input-Output Organization	6
		1

Text Books/Suggested Readings:		
S. No.	**Name of Authors/Books/Publishers**	**Year of Publication/ Repr int**
1.	Computer System Architecture: Morris M. Mano (Pearson Education)	3rd Edition
2.	Patterson and John L. Hennessy. "Computer Organization and Design: The Hardware/Software interface", Elsevier.	5th edition, 2012.

	Paper Components		
Credits	**Lecture (L)**	**Tutorial (T)**	**Practical (P)**
4	**3**	**0**	**1**
Assessment Scheme			
S.No.	**Component**	**Marking Scheme**	**Total Marks**
1	Internal Assessment		30
	• Assignment/Quiz/Project/ Presentation	12	
	• Class Test	12	
	• Attendance	6	
2.	Continuous Assessment (**Tutorial)**		NA
	• Activity 1	NA	
	• Activity 2	NA	
	• Attendance	NA	
3.	Practical		40
	• Continuous Assessment	10	
	• End Term Written/Practical Exam	20	
	• Viva	10	
4.	End Semester Examination		90